2829

Docket No.: 50090-332

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of :

Hisaya MORI, et al. :

Serial No.: 09/927,368 : Group Art Unit: 2829

Filed: August 13, 2001 : Examiner: Chan, Emily T.

For: APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT



THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

- [x] No additional fee is required.
- [ ] Applicant is entitled to small entity status under 37 CFR 1.27
- [ ] Also attached:

The fee has been calculated as shown below:

| | NO. OF CLAIMS | HIGHEST PREVIOUSLY PAID FOR | EXTRA CLAIMS | RATE | FEE |
|---|---|---|---|---|---|
| Total Claims | 11 | 20 | 0 | $18.00 = | $0.00 |
| Independent Claims | 2 | 3 | 0 | $84.00 = | $0.00 |
| | | Multiple claims newly presented | | | $0.00 |
| | | Fee for extension of time | | | $0.00 |
| | | | | | $0.00 |
| | | | | Total of Above Calculations | $0.00 |

- [ ] Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

- [x] The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

McDERMOTT, WILL & EMERY

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**Date: February 6, 2003**

U.S. Amdt A
2.13.03
C.Moore

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| Hisaya MORI, et al. | : | |
| Serial No.: 09/927,368 | : | Group Art Unit: 2829 |
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For: APPARATUS AND METHOD FOR TESTING SEMICONDUCTOR INTEGRATED CIRCUIT

**AMENDMENT**

Commissioner for Patents
Washington, DC 20231

Sir:

In response to a December 18, 2002 non-final Office Action, please amend the above-identified application as follows:

**IN THE CLAIMS:**

Please cancel claim 6.

Please amend claims 1 and 2 as follows:

1. (Amended) An apparatus for testing a semiconductor integrated circuit, comprising:

a test circuit board constructed so as to exchange a signal with a semiconductor integrated circuit under test, the semiconductor integrated circuit including an analog-to-digital converter circuit for converting an analog signal to a digital signal or a digital-to-analog converter circuit for converting a digital signal to an analog signal;

a test ancillary device disposed in the vicinity of the test circuit board, the test ancillary